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10/773,518	02/05/2004	Paul A. LaBerge	33579/US	6542

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

Edward W. Bulchis, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,518	LABERGE, PAUL A.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-40 are in the application.

Claims 1-40 are rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5,37,40 rejected under 35 U.S.C. 102 (b) as being anticipated by Doyle's (US 6229727).

As in claim 1, Doyle's describes a method of accessing a plurality of memory devices in which a plurality of terminals of a first of the memory devices (Fig 1: terminals of dram devices in #20) are interconnected with a corresponding plurality of terminals of a second of the memory devices ((Fig 1b: terminals of dram devices in #22) in a manner that causes the first and second memory devices to function differently responsive to respective address or control signals applied to the interconnected terminals, the method comprising: if the first memory device is being accessed, applying control or address signals to the interconnected terminals according to a first set of terminal assignments; and if the second memory device is being accessed, applying control or address signals to the interconnected terminals according to a second set of terminal assignments that is at least in part different from the first set of terminal assignments (Doyle's Fig 2: #16 multiplexer; Fig 6 shows the multiplexer applying addresses for first and second set of dram devices when corresponding dram devices being accessed)

As in claims 2-3,5 the claim recites wherein the parts of the first and second terminal assignments that are different comprise address terminal assignments (claim 2); wherein the parts of the first and second terminal assignments that are different comprise control terminal assignments (claim 3); wherein the memory devices comprise dynamic random access memory devices (claim 5). Doyle's Fig 1, 2 show different sockets/terminals assignments for address and control signals.

As in claim 4, the claim recites applying data signals to the interconnected terminals, and wherein the data signals are applied to the interconnected terminals according to a common set of terminal assignments regardless of whether the first memory device or the second memory

device is being accessed (Doyle's Fig 1 shows data output bus can be arraigned commonly for all dram devices).

Claim 37 rejected based on the same rationale as in the rejection of claim 1.

Claim 40 rejected based on the same rationale as in the rejection of claim 5.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-19,21,24-26,31-33,36 rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle's (US 6229727) and further in view of Jang et al (US 6667895).

As in claim 6, the claim recites a method of applying address and control signals to a plurality of identical memory devices in which a plurality of terminals of a first of the memory devices are interconnected with a corresponding plurality of terminals of a second of the memory devices in mirrored configuration, the method comprising: applying a set of control signals or a set of address signals to the interconnected terminals in a first arrangement if the first memory device is being accessed; and applying a set of control signals or a set of address signals to the interconnected terminals in a second arrangement if the second memory device is being

accessed, the second arrangement being different from the first arrangement. The claim rejected based on the same rationale as in the rejection of claim 1. Doyle does not describe the claim's detail of mirrored configuration. However, Jang describes a DIMM module with memory devices being mounted on both sides of the board. (Jang's column 1 lines 30-40). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory device in a mirrored configuration as suggested by Jang in Doyle's system thereby providing larger memory capacity while minimizing the interconnecting trace lengths (Jang's column 1 lines 28-50).

As in claim 7, the claim recites wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and second arrangements that are different from each other comprise applying a set of control signals to the interconnected terminals in first and second arrangements that are different from each other. Doyle's Fig 1 and 2 clearly shows the multiplexer #16 multiplexing address signals to different terminals of devices in #20 and #32.

As in claim 8, the claim recites wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and second arrangements that are different from each other comprise applying a set of address signals to the interconnected terminals in first and second arrangements that are different from each other. The claim rejected based on the same rationale as in the rejection of claim 7. Doyle's Fig 6 further shows a micro processor sends addresses and control signals for a particular device at time it wants to access the device.

As in claim 9, the claim recites wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and second arrangements that are different from each other comprise applying a set of both address signals and control signals to the interconnected terminals in first and second arrangements that are different from each other (Doyle's column 4 lines 9-50 clearly describes multiple configuration of memory devices, including memory devices in both banks being accessed together).

As in claim 10, the claim recites applying data signals to the interconnected terminals in a common arrangement regardless of whether the first memory device is being accessed or the second memory device is being accessed. The claim rejected based on the same rationale as in the rejection of claim 9.

Claim 11 rejected based on the same rationale as in the rejection of claim 5.

As in claim 12, the claim recites a method of applying address or control signals to a plurality of identical memory devices mounted on first and second surfaces of memory module substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface, the method comprising: coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a first configuration if the memory devices mounted on the first surface of the substrate are being accessed; and coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a second configuration that is different from the first configuration if the memory devices mounted on the second surface of the substrate are being accessed. The claim rejected based on the same rationale as in the rejection of claim 6.

As in claim 13, the claim recites wherein the acts of coupling address or control signals to the interconnected terminals in the first or second configuration comprises: coupling address or control signals to the memory module; and within the memory module, re-arranging the signals coupled to the memory module to either the first configuration or the second configuration prior to coupling the address or control signals to the interconnected terminals. Although Doyle's Fig 2 shows the multiplexer is outside the DIMM modules. However, Jang teaches an alternative embodiment in which the function of the signals multiplexing and rearranging devices pin assignments is done inside the board module (column 9 lines 35-42).

As in claim 14, the claim recites wherein the act of re-arranging the signals coupled to the memory module to either the first configuration or the second configuration comprises re-arranging the signals in a memory hub that is structured to independently access the memory devices. The claim rejected based on the same rationale as in the rejection of claim 13. Jang further shows the re-arrangement circuits, Fig 4: #450A, #450B, #480 operates parallel to the memory devices #460A, #460B.

Claim 15 rejected based on the same rationale as in the rejection of claim 7.

Claim 16 rejected based on the same rationale as in the rejection of claim 8.

Claim 17 rejected based on the same rationale as in the rejection of claim 4.

Claim 18,25,31,36 rejected based on the same rationale as in the rejection of claim 5.

As in claim 19, the claim recites a memory module, comprising: an insulative substrate; a plurality of identical memory devices mounted on first and second opposed surfaces of the insulative substrate, the memory devices being mounted on the substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first

surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface; and a memory access device mounted on the substrate, the memory access device having a plurality of terminals that are coupled through the substrate conductors to respective ones of the interconnected terminals, the memory access device being operable to receive a memory request and, in response, to couple address and control signals to the interconnected terminals for a plurality of the memory devices, the address or control signals being coupled to the interconnected terminals in a first configuration if the memory devices mounted on the first surface of the substrate are being accessed, and the address or control signals being coupled to the interconnected terminals in a second configuration that is different from the first configuration if the memory devices mounted on the second surface of the substrate are being accessed. The claim rejected based on the same rationale as in the rejection of claim 6. Jang further teaches the substrate as a layer of material used in an integrated circuit (Jang's column 3 lines 5-17).

As in claim 21, the claim recites wherein the memory access device comprises a memory hub that is structured to generate the address and control signals to access the memory devices responsive to the memory requests. The claim rejected based on the same rationale as in the rejection of claim 14.

As in claim 24, Doyle's describes the register buffer in column 5 lines 23-40.

Claim 26 rejected based on the same rationale as in the rejection of claims 13,19.

Claims 32 rejected based on the same rationale as in the rejection of claim 23.

Claims 33 rejected based on the same rationale as in the rejection of claim 19.

Claims 20,27 rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle's (US 6229727) in view of Jang et al (US 6667895) as applied to claims 13,19,26 and further in view of Bechtolsheim et al (US 5465229).

As in claim 20 the claim recites wherein the memory access device is centrally position on the insulative substrate, and wherein the memory devices are positioned to both sides of the memory access device, the memory access device being operable to couple respective sets of address or control signals in the first or second configuration to the memory devices on each side of the memory access device. Doyle and Jang do not describe the claim's detail of positioning the multiplexing circuits. However, Bechtolsheim describes a memory modules with driver circuits locate in the central of DRAM devices (Bechtolsheim's Fig 1a). It would have been obvious to one of ordinary skill in the art at the time of invention to include the signal redistributing method as taught by Bechtolsheim in Doyle's system thereby providing the routing of equally length signals to all dram devices surrounding with short sub traces, thereby minimizing the total capacitance, and increase signal rise time (Bechtolsheim's column 4 line 1-16).

Claim 27 rejected based on the same rationale as in the rejection of claim 20.

Claims 22-23,28-30,34-35,38-39 rejected under 35 U.S.C. 103(a) as being unpatentable over Doyle's (US 6229727) Jang et al (US 6667895) as applied to claims 19,26,37 and in view of Jeddeloh (US 6272609).

As in claim 22, Doyle does not describe the claim details of memory hub circuits. However, Jeddeloh describes the claim's limitation as follows:

wherein the memory hub (Jeddeloh's Fig 1) comprises: a command queue that is operable to receive the memory requests (Jeddeloh's Fig 1: #52), the memory queue further being operable to convert the memory requests into respective sets of command and address signals and to output the command and address signals in the order that the respective memory requests were received (Jeddeloh's Fig 2: #66 state machine converting request to commands and addresses for sdram device) ;

a command scheduler coupled to the command queue to receive the command and address signals from the command queue, the command scheduler arranging the timing of the command and address signals; a micro command shifter coupled to receive the command and address signals from the command scheduler after the timing of the command and address signals have been arranged (Jeddeloh's column 5 lines 5-23 state machine controls accepting requests into request queue #52 and scheduling the requests in the queue to be processed in a pipeline manner),

the micro command shifter being operable to output the command and address signals in synchronism with the operation of the memory devices (Jeddeloh's : #64 data transfer; column 4 lines 40-60),

and a multiplexer coupled to the micro command shifter to receive the command signals or the address signals from the micro command shifter, the multiplexer being operable to arrange the command or address signals in either the first configuration or the second configuration depending on whether the memory devices on the first surface or the memory devices on the second surface are being accessed, the multiplexer being operable to couple the command or address signals in either the first configuration or the second configuration to the interconnected

terminals (Jeddeloh's column 4 lines 40-60 describes two commands and addresses from decode and address modules are funneled "multiplexing" into the data transfer module). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller circuits as suggested by Jeddeloh in Doyle's system thereby allowing to process and multiplex multiple host's data requests in a pipeline manner thereby further increasing the throughput of memory transaction (Jeddeloh 's column 2 lines 2-10).

As in claim 23, the claim recites a ring buffer coupled between the multiplexer and the memory devices. Doyle's Fig 2, column 5 lines 25-53 describes the data being buffered using d-type latches.

Claims 28-29,34 rejected based on the same rationale as in the rejection of claim 22.

Claim 30,35,39 rejected based on the same rationale as in the rejection of claim 23.

Claim 38 rejected based on the same rationale as in the rejection of claims 1 and 22.

Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 3/20/06

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER